AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-26 (canceled)

27. (new) A switching power source comprising:

an inductor;

a capacitor which has one end thereof connected to one end of the inductor and another end thereof connected to a ground potential of the circuit and forms an output voltage;

a switching element which is connected to another end of the inductor and controls a current which is made to flow into the inductor based on an input voltage;

an element which brings another end of the inductor into a predetermined potential when the switching element assumes an OFF state;

a driving circuit which drives the switching element;

a booster circuit which includes a bootstrap capacity which has one end thereof connected to another end of the inductor and a MOSFET which has a source-drain route thereof connected between another end of the bootstrap capacity and an external power source terminal, and is capable of generating a boosted voltage which is used as an operating

voltage of the driving circuit on another end of the bootstrap capacity;

a level shifting circuit which forms a switching control signal which allows the MOSFET to assume an ON state when the element is in a conductive state and allows the MOSFET to assume an OFF state when the element is not in a conductive state; and

a PWM control circuit which forms a PWM signal and controls an operation of the switching element through the driving circuit, wherein

the MOSFET is configured to connect another source/drain region and a substrate gate such that a junction diode between one source/drain region and the substrate gate is directed in the direction opposite to the direction toward the external power source terminal from other end of the bootstrap capacity, and prevents the flow of the current toward the external power source terminal from another end of the bootstrap capacity by the junction diode when the boosted voltage is generated by allowing the MOSFET to assume an OFF state in response to the PWM signal.

28.(new) A switching power source according to claim 27, wherein

the switching power source includes a power source circuit which receives a high voltage corresponding to the input voltage and forms an internal voltage obtained by stepping down the high voltage, and

the internal voltage which is formed by the power source circuit is used as an operating voltage which is supplied to the booster circuit and the PWM control circuit.

29. (new) A switching power source according to claim 27, wherein the switching element and the element are formed of an N-channel MOSFET, wherein

the MOSFET of the booster circuit is formed of a P-channel MOSFET and a substrate gate of the MOSFET of the booster circuit is connected to another end of the bootstrap capacity.

30. (new) A switching power source according to claim 27, wherein

the MOSFETs of the switching element, the element and the booster circuit are formed of an N-channel MOSFET; and

a substrate gate of the MOSFET of the booster circuit is connected to the external power source terminal side.

31. (new) A switching power source according to claim 27, wherein

the switching element is formed of an N-channel MOSFET,

the element is formed of a diode; and

the MOSFET of the booster circuit is formed of a P-channel MOSFET and a substrate gate of the MOSFET of the booster circuit is connected to another end of the bootstrap capacity.

32. (new) A switching power source according to claim 30, wherein

the switching power source further includes another booster circuit which boosts an external power source voltage which is supplied from the external power source terminal, and

the level shifting circuit allows the MOSFET to assume an ON state in response to a boosted voltage of the external power source voltage which is formed by another booster circuit.

33. (new) A switching power source according to claim 29, wherein

the level shifting circuit allows the MOSFET to assume an OFF state in response to the boosted voltage which is formed by the bootstrap capacity.

34. (new) A switching power source according to claim 33, wherein

the PWM control circuit includes an error amplifier which receives a voltage signal corresponding to the output voltage and a reference voltage, a triangular wave generating circuit, a comparator which receives an output signal of the error amplifier and a triangular wave which is formed by the triangular wave generating circuit, and a control circuit which forms the PWM signal in response to an output signal of the comparator.

35. (new) A switching power source according to claim 34, wherein

the switching element, the element, the bootstrap capacity, the inductor and the capacitor are respectively formed of an external element; and

the MOSFET, the level shifting circuit, the driving circuit and the PWM control circuit are formed of one semiconductor integrated circuit, and forms a PWM signal such that the output voltage assumes the predetermined

voltage when the error amplifier of the PWM control circuit receives a voltage signal corresponding to the output voltage.

36. (new) A switching power source according to claim 34, wherein

the bootstrap capacity, the inductor and the capacitor are respectively formed of an external element; and

the switching element, the element, the MOSFET, the driving circuit, the level shifting circuit and the PWM control circuit are formed of one semiconductor integrated circuit and a PWM signal is formed such that the output voltage assumes a predetermined voltage when the error amplifier of the PWM control circuit receives a voltage signal corresponding to the output voltage.

37. (new) A switching power source according to claim 34, wherein

the bootstrap capacity, the inductor and the capacitor are respectively formed of an external element; and

the switching element, the element, the driving circuit, the MOSFET and the level shifting circuit are constituted of a first semiconductor integrated circuit; and

the control circuit is formed of a second semiconductor integrated circuit device, forms the PWM signal such that the output voltage assumes a predetermined voltage when an error amplifier of the PWM control circuit receives a voltage signal corresponding to the output voltage, and transmits a PWM signal to the first semiconductor integrated circuit.

38. (new) A switching power source according to claim 27, wherein

the switching power source further includes a power source circuit which receives a high voltage corresponding to the input voltage and forms an internal voltage which is obtained by stepping down the high voltage;

the bootstrap capacity, the inductor and the capacitor are respectively formed of an external element; and

the switching element, the element, the driving circuit, the MOSFET and the level shifting circuit are constituted of a first semiconductor integrated circuit; and

the PWM control circuit is constituted of a second semiconductor integrated circuit device, and forms the PWM signal corresponding to the high voltage such that the output voltage assumes the predetermined voltage when the PWM control circuit receives a voltage signal corresponding

to the output voltage and transmits a PWM signal to the first semiconductor integrated circuit, and

the first semiconductor integrated circuit includes a voltage clamping circuit which shifts a level of the PWM signal to amplitude between the internal voltage and the ground potential of the circuit.

39. (new) A switching power source according to claim 37, wherein

the voltage clamping circuit includes:

an input terminal to which the PWM signal is supplied;

an N-channel MOSFET which connects one of source-drain routes to the input terminal and allows a gate thereof to receive the supply of an internal voltage,

a current source which is provided between another source-drain route of the N-channel MOSFET and a ground potential of the circuit, and

a capacitor which is formed in parallel to the current source.

40. (new) A switching power source according to claim 38, wherein the first semiconductor integrated circuit includes a third semiconductor integrated circuit which constitutes the switching element, a fourth semiconductor

integrated circuit which constitutes the element, and a fifth semiconductor integrated circuit which constitutes the MOSFET and the level shifting circuit.

41. (new) A semiconductor integrated circuit comprising:

a switching element which performs a switching control of a current for forming an output voltage by stepping down an input voltage;

a first terminal which allows the current to flow therethrough;

a second terminal to which another end of a bootstrap capacity which has one end thereof connected to the first terminal is connected;

a MOSFET which has a source-drain route thereof connected between an external power source terminal and the second terminal; and

a driving circuit which drives the switching element, wherein

the bootstrap capacity and the MOSFET constitute a booster circuit for generating a boosted voltage for driving the switching element, and

the MOSFET is configured to connect another source/drain region and a substrate gate such that a

junction diode between one source/drain region and the substrate gate is directed in the direction opposite to the direction toward the external power source terminal from other end of the bootstrap capacity, and prevents the flow of the current toward the external power source terminal from another end of the bootstrap capacity by the junction diode when the boosted voltage is generated by allowing the MOSFET to assume an OFF state.

42. (new) A semiconductor integrated circuit according to claim 41, wherein

the voltage level conversion circuit is mounted on one semiconductor substrate.

43. (new) A semiconductor integrated circuit according to claim 42, wherein

the current is a current which is made to flow into an inductor which has one end thereof connected to the first terminal from the input voltage which is generated for forming the output voltage by the inductor and a capacitor which has one end thereof connected to another end of the inductor and another end thereof connected to a ground potential of the circuit.

44. (new) A semiconductor integrated circuit according to claim 43, wherein

the switching element is formed of an N-channel MOSFET, and

a MOSFET of the booster circuit is formed of a P-channel MOSFET and has a substrate gate of the MOSFET of the booster circuit is connected to another end of the bootstrap capacity.

45. (new) A semiconductor integrated circuit according to claim 43, wherein

the switching element and the MOSFET of the booster circuit are formed of an N-channel MOSFET, and

a substrate gate of the MOSFET of the booster circuit is connected to the external power source terminal side.

46. (new) A semiconductor integrated circuit according to claim 43, wherein

the semiconductor integrated circuit further includes an element which brings one terminal of the inductor into a predetermined potential when the switching element assumes an OFF state,

the element is formed on a first semiconductor substrate,

the switching element is formed on a second semiconductor substrate,

the driving circuit is a circuit which performs an ON and OFF control of the switching element and the element upon receiving a control signal which allows an output voltage to assume a desired voltage and is formed on a third semiconductor substrate, and

the first semiconductor substrate, the second semiconductor substrate and the third semiconductor substrate are sealed in one package.

47. (new) A semiconductor integrated circuit according to claim 46, wherein

the control signal is formed of a PWM signal.

48. (new) A semiconductor integrated circuit according to claim 47, wherein

the driving circuit includes a level shifting circuit which forms a switching control signal which allows the MOSFET to assume an ON state when the element is in an ON state and allows the MOSFET to assume an OFF state when the element is in an OFF state.

49. (new) A semiconductor integrated circuit according to claim 48, wherein

the PWM signal is a signal which is generated by an error amplifier which receives a voltage signal corresponding to the output voltage and a reference voltage, a triangular wave generating circuit, a comparator which receives an output signal of the error amplifier and a triangular wave which is formed by the triangular wave generating circuit, and a control circuit which receives an output signal of the comparator.

50. (new) A semiconductor integrated circuit according to claim 49, wherein

the semiconductor integrated circuit further includes a power source circuit which receives a high voltage corresponding to the input voltage and forms an internal voltage which is obtained by stepping down the high voltage, and

a voltage clamping circuit which shifts a level of the PWM signal to amplitude between the internal voltage and a ground potential of the circuit is formed in the semiconductor integrated circuit.

51. (new) A semiconductor integrated circuit according to claim 50, wherein

the voltage clamping circuit includes:

an input terminal to which the PWM signal is supplied;

an N-channel MOSFET which connects one of source-drain routes to the input terminal and allows a gate thereof to receive the supply of an internal voltage,

a current source which is provided between another source-drain route of the N-channel MOSFET and a ground potential of the circuit, and

a capacitor which is formed in parallel to the current source.

52. (new) A semiconductor integrated circuit according to claim 46, wherein

the driving circuit includes a level shifting circuit which is formed of:

a first circuit which is operated with the first amplitude;

a second circuit which includes a first MOSFET which receives a signal outputted from the first circuit, and a resistance which is connected in series with the first MOSFET between the first MOSFET and another end of the bootstrap capacity; and

a third circuit which receives a signal outputted from a node to which the first MOSFET and the resistance of the second circuit are connected and uses a voltage at another end of the bootstrap capacity as a power source, and

the driving circuit generates a control signal whose level is shifted for performing an ON and OFF control of the first switching element by discriminating a signal which is outputted from the node whose voltage level is changed by changing over ON and OFF states of the MOSFET along with a high level and a low level of the output of the first circuit in accordance with a logic threshold value of the third circuit.

53. (new) A switching power source comprising:

a first N-channel MOSFET which has a drain terminal thereof connected to a first power source terminal;

a second N-channel MOSFET which allows a source terminal and the drain terminal of the first N-channel MOSFET to be connected thereto and has a source terminal thereof connected to a ground potential terminal of the circuit;

an inductor which has one end thereof connected to the source terminal of the first N-channel MOSFET

a first capacity which has one end thereof connected to another end of the inductor and another end thereof connected to a ground potential of the circuit,

a driving circuit which drives the first and second N-channel MOSFETs,

a second capacity which has one end thereof connected to one end of the inductor; and

a MOSFET which connects a source-drain route thereof connected between another end of the second capacity and an external power source terminal, wherein

a booster circuit for generating a boosted voltage which forms a power source voltage used by the driving circuit is constituted of the second capacity and the MOSFET, and

the MOSFET is configured to connect another source/drain region and a substrate gate such that a junction diode between one source/drain region and the substrate gate is directed in the direction opposite to the direction toward the external power source terminal from another end of the second capacity.

54. (new) A switching power source according to claim 53, wherein

the switching power source prevents the flow of the current toward the external power source terminal from another end of the second capacity by the junction diode when the boosted voltage is generated by allowing the MOSFET to assume an OFF state.

55. (new) A switching power source according to claim 53, wherein

the MOSFET is formed of a P-channel MOSFET,

one of source/drain regions is connected to the external power source terminal, and

another source/drain region is connected to the second capacity.

56. (new) A switching power source according to claim 53, wherein

the MOSFET is formed of a third N-channel MOSFET,

one of source/drain regions is connected to the second capacity, and

another source/drain region is connected to the external power source terminal.

57. (new) A semiconductor integrated circuit comprising:

a first MOSFET which has one of source-drain terminals thereof connected to a first power source terminal;

a second MOSFET which allows another source-drain terminal and one of source-drain terminals of the first MOSFET to be connected thereto and has another source-drain terminal thereof connected to a ground potential terminal of the circuit;

output terminals which output currents from the first and second MOSFETs;

a driving circuit which drives the first and second N-channel MOSFETs;

an external power source terminal; and

a third MOSFET which is configured such that a source-drain route thereof is connected between an external power source terminal and another end of a first capacity which has one end thereof connected to the output terminal, wherein

the first capacity and the third MOSFET form a booster circuit which generates a boosted voltage for driving the first MOSFET, and

the third MOSFET is configured to connect another source/drain region and a substrate gate such that a junction diode between one source/drain region and the substrate gate is directed in the direction opposite to the

direction toward the external power source terminal from another end of the first capacity.

58. (new) A semiconductor integrated circuit according to claim 57, wherein

when the boosted voltage is generated, the third MOSFET assumes a non-conductive state thus preventing the flow of the current toward the external power source terminal from another end of the first capacity by the junction diode.

59. (new) A semiconductor integrated circuit according to claim 57, wherein

the third MOSFET is formed of a P-channel MOSFET,

one of source/drain regions is connected to the external power source terminal, and

another source/drain region is connected to the first capacity.

60. (new) A semiconductor integrated circuit according to claim 57, wherein

the third MOSFET is formed of an N-channel MOSFET,

one of source/drain regions is connected to the first capacity, and

another source/drain region is connected to the external power source terminal.